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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,704	HUFFMAN, WILLIAM A.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 8th of June 2004. Claims 1, 5, 6 and 9 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 8th of March 2004. Currently, claims 1-15 are pending in this application.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Trull [US 6,185,672 B1].

Referring to claim 1, Trull discloses a method of managing an arbitration queue (i.e., managing an instruction queue; See col. 5, lines 4-21) having a plurality of queue entries (i.e., a plurality of 'strings', viz., instruction storage locations; See col. 4, lines 29-30) comprising: introducing entries (i.e., new instructions) into said queue at a first, highest order queue location (i.e., "top" or start of the queue; See col. 4, lines 31-32); determining if lower order queue locations are available (See col. 26, lines 24-27); if lower order queue locations (i.e., lower order lines, where the three instructions are allocated a "line" of instruction storage locations, e.g., storage locations 200, 202, 204, 206, 208, 210 in Fig. 8A; See col. 14, lines 22-24) are available, moving all higher order queue location (i.e., all higher order lines in Figs. 8A-C) contents to an adjacent lower order queue location (i.e., adjacent lower order line of instruction storage locations 200, 202 and 204 in Figs. 8A-C) per cycle (i.e., per compression cycle; See col. 20, lines 19-38) until all lower order locations are filled (See col. 4, lines 33-42); servicing an entry (i.e., an instruction to be dispatched to processor pipe) in said queue based on servicing criteria (See col. 14, lines 36-51); and moving all higher order queue entries, with respect to an entry being serviced, to an

adjacent lower order location (i.e., lower order line) in said queue (See col. 18, line 61 through col. 19, line 24).

Referring to claim 2, Trull teaches the step of marking a location of a serviced entry (i.e., marking 'clear bit' as setting empty bit; See col. 18, lines 10-13) as idle (i.e., empty; See block 262A of Fig. 11B and col. 21, lines 63-67).

Referring to claim 3, Trull teaches said moving step further comprising for higher order locations with respect to said idle location (i.e., empty storage location), writing the contents of higher order queue locations into adjacent lower order queue locations (i.e., shift one row down; See Block 262D of Fig. 11B and col. 22, lines 19-26); and for lower order locations with respect to said idle location, rewriting the current entry into said location (i.e., no shift operation; See Block 262C of Fig. 11B and col. 22, lines 26-30; Note - the embodiment of Fig. 8A has a null logic as the new value logic in Fig. 9D).

Referring to claim 5, Trull discloses an arbitration queue circuit (i.e., instruction queue in Fig. 8A) comprising: a plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C) corresponding to a number of entries in a queue (i.e., a number of instructions in an instruction queue 314 in Figs. 8B-C; See col. 5, lines 7-10), said plurality of registers being arranged in a linear array (i.e., instruction storage locations of each column being arranged in a linear array in Figs. 8B-C) from a highest order register (i.e., a highest order storage location, e.g., storage location 236 in Figs. 8B-C) to a lower order register (i.e., a lower order storage location, e.g., storage location 200 in Figs. 8B-C); a plurality of 2:1 multiplexers (i.e., multiplexers 250 and 256 in Fig. 8A) interposed between said registers (See Fig. 8A) such that one multiplexer is interposed between a higher order register and an adjacent lower order register (e.g., a multiplexer 250 is interposed between a higher instruction storage location 206 and a subsequent instruction storage location 200 in Fig. 8A), the output of said higher order register (e.g., output from instruction storage location 206 in Fig. 8A) being coupled to a first input of said one multiplexer (i.e., an input of multiplexer 250 in Fig. 8A), the output of said adjacent lower order

register (i.e., output from instruction storage location 200 in Fig. 8A) being coupled to a second input of said one multiplexer (i.e., another input of multiplexer 250 in Fig. 8A), an output of said one multiplexer being coupled to said adjacent lower order register (i.e., an output of multiplexer 250 is coupled to instruction storage location 200 in Fig. 8A), and a mux control line (i.e., SHIFT_ROW_1 in Fig. 8A) being coupled to said one multiplexer to direct the contents of one of said first and second multiplexer inputs to said multiplexer output (See col. 18, line 63 through col. 19, line 2).

However, the recitation in the claim "whereby the mux control line associated with the higher order register and adjacent lower order register determines whether the adjacent lower order register is refreshed with its current contents or receives the contents of the higher order register" has not been given patentable weight because it has been held that the functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish. *In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).*

Referring to claim 6, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C) includes entries (i.e., new instructions) are added to said queue via said highest order register (See Figs. 3A, 3B, 11A and col. 21, lines 54-61).

Referring to claim 7, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C) each have an entry output such that an entry can be removed from any location in said queue (See col. 21, lines 37-41).

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Trull [US 6,185,672 B1] as applied to claims 1-3 and 5-7 above, and further in view of what was well known in the art, as exemplified by Garcia et al. [US 6,145,061 A; hereinafter Garcia].

Referring to claim 4, Trull discloses all the limitations of the claim 4 except that does not teach the step of initializing all queue locations to an idle state prior to the step of introducing entries into said queue.

The Examiner takes Official Notice that initializing all queue locations to an idle state prior to introducing entries into said queue, is well known to one of ordinary skill in the art, as evidenced by Garcia (i.e., initializing by zeroing all the entries prior to moving data from the old queue into a new queue; See Garcia, col. 2, line 54 through col. 3, line 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been initializing all queue locations (i.e., instruction storage locations) to an idle state (i.e., empty) prior to introducing entries into said queue (i.e., inputting instructions into instruction queue) since it would have obviate any potential malfunction by garbage data (i.e., floating data in the queue after the queue creation and/or power-on operation) in the queue.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Trull [US 6,185,672 B1] as applied to claims 1-3 and 5-7 above, and further in view of Case Law, In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.

Referring to claim 8, Trull discloses all the limitations of the claim 8 including said plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C) having 21 registers (i.e., 7 instruction storage locations) except that does not expressly teach said plurality of registers having 64 registers.

However, the claim recites said 64 registers without any patentable advantage in the specification (See claim 8 and Application page 12, lines 1-4), such as the reason of "said plurality of registers including 64 registers instead of 7 registers, 21 registers, 32 registers or 128 registers" with any patentable advantage. Therefore, the limitation of "said plurality of registers including 64 registers" in the claim is not patentably significant since it at most relates to the flexible number of registers under consideration which

is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

7. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyers et al. [US 5,375,223 A; hereinafter Meyers] in view of Trull [US 6,185,672 B1].

Referring to claim 9, Meyers discloses a computer system (i.e., multiprocessor data processing system in Fig. 1) comprising: a distributed shared memory system (i.e., main memory 300 of Fig. 1); a plurality of processors (i.e., Processors 100 in Fig. 1) generating transactions to said distributed shared memory system (See col. 3, lines 41-48); and a memory interface (i.e., memory access circuit 200 of Fig. 1) interposed between said distributed shared memory system and said plurality of processors (See Fig. 1; i.e., Memory Access circuit 200 interposed between Processors 100 and Main Memory 300 in Fig. 1), said memory interface having cache memory (i.e., Cache (L2) 220 of Fig. 1); an arbitration queue (i.e., Q 215 of Fig. 1) having a plurality of entry locations (i.e., n multi-bits positions in register 250 in Fig. 8) and a memory arbitration processor (i.e., control logic 212 of Fig. 1) for servicing transactions from said plurality of processors (See col. 4, line 61 through col. 5, line 38), said memory arbitration processor performing a memory arbitration scheme (See Fig. 2, col. 4, lines 55-60 and col. 7, line 29 through col. 8, line 32).

Meyer does not teach said arbitration queue is collapsible and said memory arbitration scheme comprising: placing transactions as entries in said arbitration queue; servicing at least one entry in said arbitration queue; marking a serviced queue entry location as idle; and collapsing said arbitration queue by bringing all higher order entries into adjacent lower order locations in said queue to fill said idle location.

Trull discloses an apparatus for instruction queue compression (See Abstract and col. 1, lines 6-8), wherein an arbitration queue (i.e., instruction queue 160 of Fig. 3A) is collapsible (i.e., compaction process; See col. 4, lines 39-42) and a memory arbitration scheme (i.e., managing an instruction queue;

See col. 5, lines 4-21) comprising: placing transactions as entries (i.e., inputting new instructions) in said arbitration queue (See col. 4, lines 31-32); servicing at least one entry in said arbitration queue (i.e., an instruction to be dispatched to processor pipe; See col. 14, lines 36-51); marking a serviced queue entry location (i.e., marking 'clear bit' as setting empty bit; See col. 18, lines 10-13) as idle (i.e., empty; See block 262A of Fig. 11B and col. 21, lines 63-67); and collapsing said arbitration queue (i.e., compaction process) by bringing all higher order entries (i.e., all higher order instructions in Figs. 8A-C) into adjacent lower order locations (i.e., adjacent lower order lines of instruction storage locations composed of 3 columns in Figs. 8A-C) in said queue to fill an idle location (i.e., shifting down to adjacent lower order line and filling empty location; See col. 18, line 61 through col. 19, line 24).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said collapsible arbitration queue and said memory arbitration scheme, as disclosed by Trull, for said arbitration queue and memory arbitration scheme, as disclosed by Meyer, for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of said idle locations (i.e., empty storage locations; See Trull, col. 3, lines 48-62 and col. 4, lines 20-23).

Referring to claim 10, Trull teaches said collapsing operation comprises: for higher order queue locations with respect to said idle location (i.e., empty storage location), writing the contents of higher order queue locations into adjacent lower order queue locations (i.e., shift one row down; See Block 262D of Fig. 11B and col. 22, lines 19-26); and for lower order queue locations with respect to said idle location, rewriting the current entry into said location (i.e., no shift operation; See Block 262C of Fig. 11B and col. 22, lines 26-30; Note - the embodiment of Fig. 8A has a null logic as the new value logic in Fig. 9D).

Referring to claim 11, Trull teaches said plurality of entry locations (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B) includes a highest order location (i.e., instruction storage locations 236, 238, 240 in Fig. 8B) and a lowest order location (i.e., instruction storage locations 200, 202, 204 in Fig. 8B), and wherein entries (i.e., new instructions) are added to said queue via said highest order location (See Figs. 3A, 3B, 11A and col. 21, lines 54-61).

Referring to claim 12, Trull teaches said arbitration queue (i.e., instruction queue 160 of Fig. 3A) comprising a plurality of registers (i.e., instruction storage locations 200, 202, 204, 206, 208, 210 in Fig. 8A) corresponding to the number of entries in said queue (See col. 5, lines 7-10); a plurality of 2:1 multiplexers (i.e., multiplexers 250, 252, 254, 256, 258, 260 in Fig. 8A) interposed between said registers (See Fig. 8A) such that one multiplexer is interposed between a higher order register and a subsequent register (e.g., a multiplexer 250 is interposed between a higher instruction storage location 206 and a subsequent instruction storage location 200 in Fig. 8A), the output of said higher order register (e.g., output from instruction storage location 206 in Fig. 8A) being coupled to a first input of said one multiplexer (i.e., an input of multiplexer 250 in Fig. 8A), the output of said subsequent register (i.e., output from instruction storage location 200 in Fig. 8A) being coupled to a second input of said one multiplexer (i.e., another input of multiplexer 250 in Fig. 8A), an output of said one multiplexer being coupled to said subsequent register (i.e., an output of multiplexer 250 is coupled to instruction storage location 200 in Fig. 8A), and a mux control line (i.e., SHIFT_ROW_1 in Fig. 8A) being coupled to said one multiplexer to direct the contents of one of said first and second multiplexer inputs to said multiplexer output (See col. 18, line 63 through col. 19, line 2).

However, the recitation in the claim "whereby the mux control line associated with the higher order register and subsequent register determines whether the subsequent register is refreshed with its current contents or receives the contents of the higher order register" has not been given patentable weight

because it has been held that the functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish. *In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).*

Referring to claim 13, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B) includes a highest order register (i.e., instruction storage locations 236, 238, 240 in Fig. 8B) and a lowest order register (i.e., instruction storage locations 200, 202, 204 in Fig. 8B), and wherein entries (i.e., new instructions) are added to said queue via said highest order register (See Figs. 3A, 3B, 11A and col. 21, lines 54-61).

Referring to claim 14, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B) each have an entry output such that an entry can be removed from any location in said queue (See col. 21, lines 37-41).

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meyers [US 5,375,223 A] in view of Trull [US 6,185,672 B1] as applied to claims 9-14 above, and further in view of Case Law, In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.

Referring to claim 15, Meyers, as modified by Trull, discloses all the limitations of the claim 15 including said plurality of registers (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B; Trull) having 21 registers (i.e., 21 instruction storage locations; Trull), except that does not expressly teach said plurality of registers having 64 registers.

However, the claim recites said 64 registers without any patentable advantage in the specification (See claim 15 and Application page 12, lines 1-4), such as the reason of "said plurality of registers including 64 registers instead of 21 registers, 32 registers or 128 registers" with any patentable advantage. Therefore, the limitation of "said plurality of registers including 64 registers" in the claim is not patentably significant since it at most relates to the flexible number of registers under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Response to Arguments

9. Applicant's arguments filed on 8th of June 2004 (hereinafter the Response) have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "Claims 1-3 and 5-7 stand rejected under 35 U.S.C. §102(e) as being anticipated by Trull. ... By contrast, the Trull patent moves contents of particular higher order queue locations to non-adjacent lower order queue locations. Thus, the Trull patent does not move all higher order queue location contents to an adjacent lower order queue location as required by the claimed invention. With respect to Independent Claim 5, there is recited '... a plurality of 2:1 multiplexers interposed between said registers such that one multiplexer is interposed between a higher order register and an adjacent lower order register ...' By contrast, the Trull patent merely shows 2:1 multiplexers disposed between rows of storage locations in an instruction queue so that the contents of one location can be placed three locations away. Thus, the Trull patent does not use 2:1 multiplexers to move register contents from a higher order register to an adjacent lower order register as required by the claimed invention. ..." on the Response page 7, lines 7-30, the Examiner respectfully disagrees.
In contrary to the Applicant's statement, Trull suggests moving all higher order queue location (i.e., all higher order lines in Figs. 8A-C) contents to an adjacent lower order queue location (i.e., adjacent lower order line of instruction storage locations 200, 202 and 204 in Figs. 8A-C) per cycle (i.e., per compression cycle; See col. 20, lines 19-38) until all lower order locations are filled (See col. 4, lines 33-42). Moreover, as admitted by the Applicant, Trull shows 2 a plurality of 2:1 multiplexers (i.e., multiplexers 250 and 256 in Fig. 8A) interposed between rows of storage locations (i.e., registers; See Fig. 8A). And, Trull clearly suggests that one multiplexer is interposed between a higher order register and an adjacent lower order register (e.g., a multiplexer 250 is interposed between a higher instruction storage location 206 and a subsequent instruction storage location 200 in Fig. 8A). And, in contrary to the Applicant's assertion, such that Trull merely shows 2:1 multiplexers disposed between rows of storage locations in an

instruction queue so that the contents of one location can be placed three locations away, Trull's each of the plural 2:1 multiplexers is disposed between adjacent storage locations in an instruction queue, respectively, so that the contents of one location (e.g., higher instruction storage location 206 of Fig. 8A) can be placed an adjacent location (i.e., a subsequent instruction storage location 200 of Fig. 8A), which is not located three locations away, but adjacently located at its higher instruction storage location. Refer to the instant Office Action, paragraph 3, claims 1-3 and 5-7 rejection under 35 U.S.C. 102(e) as being anticipated by Trull.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Claims 9-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Meyers et al. in view of Trull. ... However, the Trull patent moves particular contents of particular higher order queue locations to non-adjacent lower order queue locations. Thus, the Trull patent does not move all higher order entries to adjacent lower order locations as required by the claimed invention. ..." on the Response page 8, lines 16-32, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, Trull suggests collapsing said arbitration queue (i.e., compaction process) by bringing all higher order entries (i.e., all higher order instructions in Figs. 8A-C) into adjacent lower order locations (i.e., adjacent lower order lines of instruction storage locations composed of 3 columns in Figs. 8A-C) in said queue to fill an idle location (i.e., shifting down to adjacent lower order line and filling empty location; See col. 18, line 61 through col. 19, line 24).

Furthermore, the claim 9 rejection under *35 USC §103(a)* in the prior and the instant Office Action established a *prima facie* case of obviousness meeting the three basic criteria of the M.P.E.P. 2143.03 (8th ed. 2001). And, the Examiner has clearly pointed out rationale for appropriate combination of the references Meyers and Trull. Refer to the instant Office Action, paragraph 7, claims 9-14 rejection under 35 U.S.C. 103(a) as being unpatentable over Meyers in view of Trull.

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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cel/

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